AMENDMENTS TO THE SPECIFICATION

I. Please replace the last paragraph on page 1, which starts with "This and other needs are satisfied..." with the following amended paragraph.

This and other needs are satisfied by the present invention which provides a method of synthesizing a register transfer level (RTL) based design of a system. The method comprises the steps of determining sub-modules of a top-level system and determining individual time budgets for each sub-module based on timing requirements of the top-level system. ~~Gate-level~~ Gate level designs of the sub-modules are synthesized based on the determined time budgets for the individual sub-modules. The ~~gate-level~~ gate level designs of the individual sub-modules are integrated to form a top-level design. The top-level design is tested for conformance with top-level design requirements. A top-level netlist is generated when the top-level design conforms to the top-level designer requirements.

II. Please replace the first full paragraph on page 2, which starts with "By performing this "bottom-up" approach..." with the following amended paragraph.

By performing this "bottom-up" approach towards synthesizing the RTL based design, the ~~logic~~ gate level design of sub-modules can be synthesized independently as a stand-alone design more efficiently and achieve a better area optimization while at the same time meeting the logic functionality and speed of operation requirements of the whole design. Also, the breaking up of the large and complex top-level design into a few logical sub-modules or sub-blocks permits the achievement of a quick turn-around time for design to meet the fast time-to-market requirements of integrated circuit innovations.

III. Please replace the seventh paragraph on page 2, which starts with "The present invention addresses and solves problems..." with the following amended paragraph.

The present invention addresses and solves problems associated with the synthesis of RTL based design from a top-level design while meeting the timing constraints in a fast and efficient manner. This is achieved in the present invention through a bottom-up approach toward the synthesis of the RTL based design. In such an approach, a large and complex design is divided into a plurality of logical sub-modules of block designs. ~~These logic~~ The gate level design ~~modules~~ of these sub-modules are synthesized independently as stand-alone designs in a more efficient manner. A better area of optimization is achieved, while meeting the logical functionality and speed of operation requirements of the whole design.

IV. Please replace the second paragraph on page 3, which starts with "Figure 2 is a block diagram depicting the breakdown..." with the following amended paragraph.

Figure 2 is a block diagram depicting the breakdown of a top-level synthesis to a sub-module synthesis for the bottom-up approach of synthesis of RTL based design in accordance with embodiments of the present invention. In the present invention, the timing requirements of the top-level design are determined, in block 20. These timing requirements for the top-level design are used in the synthesis of the top-level RTL based design in block 22. In conventional approaches, the top-level RTL is then used to synthesize the top-level design of the integrated circuit. From the synthesis of the top-level design provided in block 24, ~~the gates~~ a netlist of the top-level design ~~are~~ is provided, ~~in a netlist,~~ as depicted in block 36. The dashed lines in Figure 2 represent the prior art approach to the synthesis of an RTL based design using a top-level synthesis flow, instead of the bottom-up approach of the present invention.

V. Please replace the previously amended third paragraph on page 4 which starts with "Figure 3 depicts a typical flow..." with the following amended paragraph.

Figure 3 depicts a typical flow of the synthesis of ~~an RTL-based~~ a gate level design for a sub-module, as depicted by blocks 32A, 32B and 32C in Figure 2. This synthesis ~~of an RTL-based design~~ may be used for top-level designs or for individual sub-module designs. The synthesis finds particular application in the present invention for synthesizing sub-modules, which are then integratable into a top-level design, rather than using the synthesis to directly synthesize the top-level design.

VI. Please replace the fourth paragraph on page 4, which starts with "In the typical flow of...", with the following amended paragraph.

In the typical flow of synthesis of ~~an RTL-based~~ a gate level design for a sub-module, the synthesis/optimization process is represented by block 46 and receives as inputs the timing requirements of the design 40 for that sub-module, RTL design 42 for that ~~logic~~ sub-module, and the wire loading and I/O loading/drivers 44 for that ~~logic~~ sub-module. The synthesis/optimization process uses these inputs to generate the ~~logic~~ gate level design ~~and a logic gate netlist for the sub-module. This is~~ as depicted in blocks 46 and 48. Based upon the ~~logic~~ gate level design, verification is performed and is represented by block 50. The verifications include a static timing analysis 52, dynamic simulation of the circuitry 54, and other formal verifications typically used in RTL-based design. When the requirements are met, as depicted by decision block 58, the ~~RTL~~ synthesis ~~and timing optimization for~~ of gate level design of the sub-module is complete and ready for production of a netlist for that sub-module. Referring back to Figure 2, the sub-module netlist for that sub-module may then be integrated

with the other sub-module netlists to form a top-level netlist for the top-level design. If the requirements are not met, the process returns back to one of the previous process steps, depending on which requirements are not met. The process is iterated to optimize or re-synthesize to meet the timing requirements for that sub-module.

VII. Please replace the first paragraph on page 5, which starts with "When the verifications are passed, the top-level ..." with the following amended paragraph.

When the verifications are passed, the top-level netlist is fed to a back-end process where the top-level netlist is placed and routed. When the place and route process is completed, more accurate extracted information is used in the synthesis of the ~~sub-module levels~~ gate level design of the sub-modules to provide final and more accurate optimizations. The synthesis of the gate level design of the sub-modules is repeated to achieve the final top-level design that meets all the timing requirements and functional specifications of the top-level design.

VIII. Please replace the previously amended second and third paragraphs on page 5 which starts with "The procedures described above are summarized..." with the following amended paragraph.

The procedures described above are summarized in the flow chart of Figure 4 in which the top-level timing requirements are provided in step 60. The time-budget of each of the sub-modules determines the timing requirements for each of the sub-modules, as provided in step 62. Each of the sub-modules undergoes independent ~~gate-level~~ gate level synthesis in steps 64A-C. The ~~gate-level~~ gate level design synthesis for the sub-module ~~design~~ is based on the timing requirements, wire load modules, and I/O signal loadings, for example. Verification of the

performance of the ~~gate-level~~ gate level design of the sub-modules ~~are~~ is performed in steps 65A-C. These include static timing analysis, dynamic simulations and other formal verifications. It is then determined in steps 66A-C~~,~~ for each of the sub-modules, whether the timing requirements for the sub-modules are met. If they are not met, the synthesis process of gate level design for the individual sub-module or sub-modules is/are performed until the timing requirements are met and verifications passed.

Once an individual sub-module has passed the timing requirements and verifications, as determined in steps 66A-C, a ~~gate-level~~ netlist for that gate level design is provided in steps 68A-C, which are ~~to be~~ integrated in step 70 with the other ~~gate-level~~ netlists for the corresponding gate level designs of the other sub-modules to form ~~a~~ an integrated top-level design netlist. The integrated top-level design netlist for the corresponding gate level designs of all the sub-modules is then tested in step 71 in the same manner as each of the individual sub-modules in steps 65A-C. It is determined in step 72 whether the integrated top-level netlist ~~and design~~ for the corresponding gate level designs of all the sub-modules satisfies all of the top-level designed timing requirements and other verifications performed on the top-level final design. If it does not, the process returns to step 62 or steps 64A-C to re-perform the synthesis of the gate level design for the sub-modules.

IX. Please replace the fourth paragraph on page 5, which starts with "When the final integrated the top-level design..." with the following amended paragraph.

When the ~~final~~ integrated top-level design netlist for the corresponding gate level designs of all the sub-modules passes the verification procedure, as determined in step 72, a top-level netlist ~~is fed through the back-end process where the top-level netlist~~ is generated (step 74) and

then placed and routed (step 76). Once the place and route process is completed, more accurate extracted information is used to impose on the sub-module synthesis to produce a final and more accurate optimization of the design. This is depicted by the determination in step 78 whether the optimization is finalized. If the optimization is considered to be a final optimization, the process is exited.